What is claimed:

1. A semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer.

2. A semiconductor device according to claim 1, wherein the first semi-recessed LOCOS layer and the second semi-recessed LOCOS layer each have a thickness of 0.3 – 0.7 μm.

3. A semiconductor device according to claim 1, further comprising an element isolation region, wherein the element isolation region has a semi-recessed LOCOS structure.

4. A semiconductor device according to claim 3, wherein a channel stopper layer is provided below the element isolation region.

5. A semiconductor device according to claim 1, wherein a low concentration impurity layer having a conductivity type identical with conductivity type of the drain region is provided adjacent to the drain region.

6. A method for manufacturing a semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi-recessed LOCOS layer is to be formed

implanting an impurity in a semiconductor substrate in the first recessed section and in the second recessed section; and

thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section.

7. A method for manufacturing a semiconductor device according to claim 6, further comprising forming an anti-oxidation layer having a predetermined pattern, wherein the thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section is conducted using the anti-oxidation layer formed on the semiconductor substrate as a mask.

8. A method for manufacturing a semiconductor device according to claim 7, wherein the anti-oxidation layer has a film thickness of 50 – 70 nm.

9. A method for manufacturing a semiconductor device according to claim 7, further comprising, before the forming of the anti-oxidation layer, forming a protection film over the semiconductor substrate in the first recessed section and in the second recessed section.

10. A method for manufacturing a semiconductor device according to claim 9, wherein the protection film is a silicon oxide layer.

11. A method for manufacturing a semiconductor device according to claim 10, wherein the silicon oxide layer is formed by a thermal oxidation method.

12. A method for manufacturing a semiconductor device according to claim 9, further comprising, after the implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section, removing the protection film.

13. A method for manufacturing a semiconductor device according to claim 6, wherein the first recessed section and the second recessed section each are formed in a tapered configuration.

14. A method for manufacturing a semiconductor device according to claim 13, wherein a tapered angle of each of the first recessed section and the second recessed section is 60 degrees or greater less than 90 degrees.

15. A method for manufacturing a semiconductor device according to claim 6, wherein an implanting direction of the impurity traverses a normal line of a surface of the semiconductor substrate during the implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section.

16. A method for manufacturing a semiconductor device according to claim 15, wherein the implanting direction of the impurity and the normal line of the surface of the semiconductor substrate define an angle that is greater than zero degrees and no greater than 45 degrees.

17. A semiconductor device comprising:

first and second field effect transistors each including a gate dielectric layer; source and drain regions; a first semi-recessed LOCOS layer positioned between the gate dielectric layer and the drain region; a second semi-recessed LOCOS layer positioned between the gate dielectric layer and the source region; a first offset impurity layer below the first semi-recessed LOCOS layer; and a second offset impurity layer below the second semi-recessed LOCOS layer; and

an element isolation region located between the first and second field effect transistors.

18. A semiconductor device according to claim 17, wherein said element isolation region includes a semi-recessed LOCOS structure.

19. A semiconductor device according to claim 17, further comprising a channel stopper layer formed below the element isolation region.

20. A liquid crystal display driver comprising the semiconductor device of claim 17.